Action, however, rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 102(e) as allegedly

unpatentable over U.S. Patent 5,844,818 to Kochpatcharin et al. Applicant respectfully

traverses the rejections and requests reconsideration and withdrawal of all rejected claims.

Summary

The present application is directed to a method and apparatus for evaluating a gate of

an integrated circuit to determine whether or not the gate has acceptable immunity to noise.

The apparatus comprises a computer configured to execute a rules checker program, which

receives input relating to characteristics of a static gate contained in the integrated circuit.

The gate comprises at least two field-effect transistors (FETs). Each FET has a width and the

characteristics received in the input to the rules checker program include the widths of the

field effect transistors. The rules checker program analyzes the widths of the FETs to

determine whether or not the gate has an acceptable noise immunity.

Each gate typically comprises a plurality of FETs, usually an NFET and a PFET, and

input terminals for receiving input signals. The rules checker program processes the widths

of the PFETs and NFETs to obtain at least a first numerical value relating to the widths. The

rules checker program utilizes the first numerical value to access one or more threshold noise-

level values from a memory device in communication with the computer. The rules checker

program determines noise levels on the inputs, either through calculation or simulation. The

rules checker program compares the determined noise levels with the threshold values and

uses the results of the comparison to determine whether or not the gate has an acceptable

immunity to noise.

Discussion of Office Action Rejections

A Fundamental Distinction of the Kochpatcharin Patent

Applicant respectfully traverses the rejections of the claims of the present application based upon Kochpatcharin, for reasons that will be specifically discussed below. However, before addressing the details of the specific rejections, Applicant notes that there are fundamental differences between the system of Kochpatcharin and the present invention. As summarized above, the present invention is directed to a method for evaluating a gate node to determine whether the gate node has been designed to have an acceptable level of noise immunity. Specifically, and as expressly set forth in the claims of the present application, the present invention performs this by analyzing widths of transistors in the gate node.

The Kochpatcharin patent, however, is completely devoid of any such teaching. Instead, the Kochpatcharin patent is directed to a system for evaluating functional blocks of an IC design. More particularly, the system of Kochpatcharin creates "shells" that retain critical information from a functional block of an IC design, and later uses those shells in a static rules-checking procedure (see col. 1, lines 40-49). Significantly, Kochpatcharin wholly fails to even mention such low-level devices as transistors, much less disclose the evaluation of transistor widths for purposes of assessing noise immunity.

In fact, the undersigned attorney performed an electronic search of the entire text of the Kochpatcharin patent for the terms "noise," "transistor," and "width" and confirmed that none of these terms are used anywhere in that patent. Consequently, without using such terms, which are so fundamental to the broad inventive concepts of the present invention, there can clearly be no anticipation of the specifically-claimed features.

Discussion of Specific Rejections based upon Kochpatcharin

Turning now to the specific rejections, the Office Action rejected claims 1, 2, 8, 9, 15, and 16 under 35 U.S.C. § 102(e), as being anticipated by Kochpatcharin et al. Applicant respectfully traverses this rejection for at least the reasons that follow.

In rejecting claims 1 and 15, the Office Action states:

> As per claims 1 and 15, Kochpatcharin anticipates method and system for design rule checking of an integrated circuit design with feature limitations as claimed (Abstract and Summary of the Invention). According to Kochpatcharin, the method and system for design rule checking includes a computer configured to execute a rule checker program, wherein the design rule being checked for an integrated circuit design having gates, gate connected in datapath or along circuit paths including static gate characteristics, transistor parameters such as transistor widths, lengths, connected in device channel, etc. ("Summary of the Invention", col. 6, lines 19-51, for instance). The program is designed to check transistor susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5, lines 18-56, col. 4, line 5 to col. 6, line 60, for example), including checking noise susceptible or noise immunity as claimed for transistors to other transistors as claimed for design practice adherence or design quality as suggested use for in the Background of the Invention.

The undersigned has closely reviewed the Kochpatcharin reference and submits that it does not disclose the invention as defined by the independent claims of the present application.

Turning first to independent claim 1, independent claim 1 recites:

> 1.   An apparatus *for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise*, the apparatus comprising:
>   a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, *the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity*.

Likewise, claim 15 recites:

> 15.   A computer-readable medium containing a rules checker computer program, the computer program *evaluating a gate to determine whether or not the gate has an acceptable immunity to noise*, the gate comprising at least two field effect transistors, each field effect transistor having a

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width, the characteristics including the widths of the field effect
transistors, the program comprising:
> *code which analyzes the widths of the field effect transistors to*
> *determine whether or not the gate has an acceptable noise immunity.*

(*Emphasis added.*) Applicant respectfully traverses the rejection of claims 1 and 15 for at least the reason that Kochpatcharin fails to disclose or teach at least the features emphasized above.

As set forth above, Kochpatcharin is directed to a system for evaluating functional blocks of an IC design. In contrast, claim 1 specifies the *analysis of widths of field effect transistors within a static gate*, to determine whether the gate has an acceptable *noise immunity* (claim 15 includes similar features). Simply stated, Kochpatcharin does not teach this claimed aspect, and therefore cannot form a proper anticipatory reference. Furthermore, the undersigned performed an electronic search of the entire text of the Kochpatcharin patent for the individual terms "noise," "transistor," and "width." None of these terms are mentioned or used anywhere within the Kochpatcharin patent. Consequently, the Kochpatcharin patent cannot anticipate claim 1 or 15 of the present application.

Further, the Office Action cited the Summary of the Invention and col. 6, lines 19-51 of Kochpatcharin as allegedly teaching the claimed portion of the rules checker program that analyzes the widths of FETs to determine whether or not the gate has an acceptable level of noise immunity. As is verified from even a cursory review of this portion of Kochpatcharin, no such teaching is present. Instead, the cited portion of Kochpatcharin teaches only a system that creates "shells" that retain critical information from a functional block of an IC design, and later uses those shells in a hierarchical static rules-checking procedure.

For at least the foregoing reasons, Applicant respectfully submits that the rejection of claims 1 and 15 is misplaced and should be withdrawn. For at least these same reasons,

claims 2 and 16, which depend from claims 1 and 15, respectively, patently define over

Kochpatcharin as well.

Claims 8 and 9

The Office Action also rejected claims 8 and 9 under 35 U.S.C. § 102(e), as being

anticipated by Kochpatcharin. Applicant respectfully traverses this rejection for at least the

reasons that follow.

Independent claim 8 recites:

> 8.　　A method *for evaluating a gate to determine whether or not the*
> *gate has an acceptable immunity to noise,* the method comprising the steps
> of:
> 　　　receiving input in a computer relating to characteristics of a static
> gate contained in the integrated circuit, the gate comprising at least two field
> effect transistors, each field effect transistor having a width, the
> characteristics including the widths of the field effect transistors; and
> 　　　*analyzing the widths of the field effect transistors in the computer*
> *to determine whether or not the gate has an acceptable noise immunity,*
> *wherein the computer executes a rules checker program which analyzes*
> *the widths to determine whether or not the gate has an acceptable noise*
> *immunity.*

(*Emphasis added.*) Applicant respectfully traverses the rejection of claim 8 for at least the

reason that Kochpatcharin fails to disclose or teach either of the features emphasized above.

The Office Action rejected claim 8 stating only:

> As per claim 8, Kochpatcharin anticipates method for design rule
> checking of an integrated circuit design with feature limitations as claimed
> (Abstract and Summary of the Invention). According to Kochpatcharin, the
> design rule checking method includes steps for receiving gate characteristics
> such as width and length of the design gate parameter for static gate rule
> checking, wherein the design gate usually contained more than one field
> effect transistor, and the gates connected in datapath or along circuit paths
> including static gate characteristics in which the gate characteristics
> involving with transistor parameters such as transistor widths, lengths,
> connected in device channel, etc. ("Summary of the Invention", col. 6, lines
> 19-51, for instance). The rule checking method is to check transistor
> susceptible to noise in the cross-talk influence (col. 2, lines 7-24, col. 5,
> lines 18-56, col. 4, line 5, lines 18-51, col. 6, lines 20-51), including
> checking noise susceptible or noise immunity as claimed for transistors to

other transistors as claimed for design practice adherence or design quality as suggested use for in the background of the invention.

As can be readily verified from even a cursory review of the cited portions of Kochpatcharin, this cited portion does not disclose a step of *"analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity,"* which is specifically claimed in claim 8.

As noted above in connection with claim 1, Kochpatcharin is directed to a system for evaluating functional blocks of an IC design. Further, the cited portion of Kochpatcharin teaches only a system that creates "shells" that retain critical information from a functional block of an IC design, and later uses those shells in a hierarchical static rules-checking procedure.

Consequently, and for the same reasons set forth in connection with claim 1, Applicant respectfully submits that the rejection of claims 8 is misplaced and should be withdrawn. For at least these same reasons, claim 9, which depends from claim 8, patently defines over Kochpatcharin as well.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to Hewlett-Packard Company's deposit account No. 08-2025.

Respectfully submitted,

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By:_____

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